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Applicant(s)	William R. Young	<b>TRANSMITTAL FORM UNDER 37 CFR 1.8 (LARGE ENTITY)</b>
Serial No.	10/076,716	
Filing Date	February 14, 2002	
Group Art Unit	2837	
Examiner Name	Anthony J. Salata	
Attorney Docket No.	125.010US01	
Title: ESD PROTECTION NETWORK UTILIZING PRECHARGE BUS LINES		

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Name	Scott V. Lundberg	Signature			



**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE  
BEFORE THE BOARD OF PATENT APPEALS**

Appellant:	William R. Young	<b>APPEAL BRIEF</b>
Serial No.	10/076,716	
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**1. Introduction**

On March 8, 2004, Appellants filed a notice of appeal from the final rejection of claims 1, 2, 4-16, 22, 26-31, 33, 34 and 46-48 set forth in the Final Office Action mailed January 6, 2004. Three copies of this Appeal Brief are hereby timely filed on May 11, 2004 and are accompanied by a fee in the amount of \$330.00 as required under 37 C.F.R. §1.17(c).

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**2. Real Party in Interest**

The real party in interest in the above-captioned application is the assignee Intersil Americas Inc.

**3. Related Appeals and Interferences**

There are no other appeals or interferences known to Appellants that will have a bearing on the Board's decision in the present appeal.

**4. Status of the Claims**

Claims 1-57 are pending in this application and claims 1, 2, 4-16, 22, 26-31, 33, 34 and 46-48 are subject of this appeal. In a final office action mailed January 6, 2004, claims 1, 2, 4, 5, 14-16 and 46-48 were finally rejected under 35 U.S.C. §102(b); claims 6-9, 10-13, 22, 26-31, 33 and 34 were finally rejected under 35 U.S.C. §103(a). Claims 17-21, 23-25, 32, 35 and 49 were objected to and claims 36-45 and 50-57 were allowed.

**5. Summary of the Amendments**

No amendment has been filed subsequent to the Final Office Action mailed January 6, 2004.

**6. Summary of the Invention**

In one embodiment, an electrostatic discharge protection circuit is disclosed. An example of an invention of this embodiment is illustrated in Figure 1 and described in paragraphs [0026] – [0039] of the present application. The electrostatic discharge protection circuit 100 includes one or more electrostatic bus lines 45 and 47, a plurality of signal bonding pads 14 and 22 and a charge pump 120 and 122 for each electrostatic bus line 45 and 47. The one or more

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electrostatic bus lines 45 and 47 are used to direct electrostatic discharge around internal circuitry 28. The plurality of signal bonding pads 14 and 22 are used to receive external voltage signals. Each signal bonding pad 14 and 22 is coupled to an associated electrostatic bus line 45 and 47 via an unidirectional conducting device 10, 20, 16, and 24. Each charge pump 120 and 122 is used to precharge its associated electrostatic bus line 45 and 47 to an associated predetermined voltage level. The pre-charging of each electrostatic bus line 45 and 47 to its predetermined voltage level reduces transient currents on the signal bonding pads 14 and 22 associated with capacitive charging of the electrostatic bus lines 45 and 47 when the external voltage signals levels are beyond normal supply voltage ranges.

In another embodiment an integrated circuit comprises functional circuitry, first and second ESD bus lines, first and second charge pumps and first and second unidirectional conducting devices. An example of an invention of this embodiment is also illustrated in Figure 1 and described in paragraphs [0026] – [0039] of the present application. The first ESD bus line 45 is used to direct electrostatic discharge pulses away from the functional circuitry 28. The first charge pump 120 is coupled to charge the first ESD bus line 45 to a predetermined first voltage. The second ESD bus line 47 is used to further direct electrostatic discharge pulses away from the functional circuitry 28. The second charge pump 122 is coupled to charge the second ESD bus line 47 to a predetermined second voltage. The first unidirectional conducting device 10 is coupled between a first signal connection 14 and the first ESD bus line 45. The second unidirectional conducting device 24 is coupled between a second signal connection 22 and the second ESD bus line 47. The first and second ESD bus lines 45 and 47 are charged to their respective first and second voltage levels to reduce transient currents through the first and second unidirectional conducting devices 10 and 24 when voltages applied to the first and second signal connections 14 and 22 are outside the normal range of power supply operating voltages for the integrated circuit 28.

In another embodiment, an ESD protected integrated circuit comprises a positive ESD bus line, first and second signal bonding pads, a first unidirectional conducting device, a second

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bus line, a second unidirectional conducting device and a positive rail charge pump. An example of this embodiment is illustrated in Figure 3 which described in paragraphs [0040] – [0044] of the present application. The positive ESD bus line 45 is used to route positive electrostatic discharge pulses around functional circuitry 28. The first and second signal bonding pads 14 and 22 are used to receive external voltage signals. The first unidirectional conducting device 130 is coupled between the first signal bonding pad 14 and the positive ESD bus line 45. The second bus line 21 is coupled to selectively receive current from the positive ESD bus line 45. The second unidirectional conducting device 132 is coupled between the second signal bonding pad 22 and the second bus line 21. The positive rail charge pump 120 is coupled to charge the positive ESD bus line 45 to a predefined voltage level, wherein the predefined voltage level is higher than anticipated voltage signal levels that will be applied to the first signal bonding pad 14 to reduce parasitic currents through the first unidirectional conducting device 130 during normal operations of the integrated circuit 28 where voltage signals higher than a normal power supply operating voltage, but less than the predefined voltage signals, are applied to the first signal bonding pad 14.

In another embodiment, a method of operating an integrated circuit that requires signal voltages outside the normal range of power supply operational voltages, the integrated circuit including an electrostatic discharge circuit having one or more electrostatic discharge bus lines. This method is described in paragraph [0034] of the present application. The method comprising, pre-charging each of the electrostatic discharge bus lines to a respective predetermined voltage level, wherein each predetermined voltage level is a voltage level beyond the signal voltage level expected to be applied to the integrated circuit.

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**7. Issues Presented for Review**

Whether the Examiner erred in rejecting Independent claims 1, 14 and 46 under 35 U.S.C. 102(b) as being anticipated by Smith et al. (U.S. Patent # 6,046,897) and claim 26 under 35 U.S.C. 103(a) as being unpatentable over Smith et al and Ker et al (U.S. Patent # 6,144,542).

**8. Grouping of Claims**

Each of claims 1, 2, 4-16, 22, 26-31, 33, 34 and 46-48 stand or fall on their own merits. However, in the desire for brevity, only the rejected independent claims (claims 1, 14, 26 and 46) are addressed in this appeal. Therefore, in regards to this appeal, the rejected dependant claims stand or fall on their related independent claims.

**9. Argument****A. Scope and Content of Prior Art**

The Examiner has cited the Smith et al. (U.S. Patent No. 6,046,897) reference, and the Ker et al. (U.S. Patent No. 6,144,542).

The Smith et al. reference relates to segmented bus architecture for electrostatic discharge protection.

The Ker et al. reference related to an electrostatic discharge bus line in CMOS integrated circuits for whole chip electrostatic discharge protection.

**B. Rejection of Claims 1, 14 and 46 under 35 U.S.C. §102(b)****i. The Applicable Law**

35 U.S.C. § 102 provides in relevant part:

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A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in a public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

A claim is anticipated under 35 U.S.C. § 102 only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.

*Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). “The identical invention must be shown in as complete detail as is contained in the . . . claim.” *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim, but identical terminology is not required. *In re Bond*, 910 F. 2d 831, 15 U.S.P.Q.2d 1566 (Fed. Cir. 1990).

Anticipation focuses on whether a claim reads on a product or process disclosed in a prior art reference, not on what the reference broadly teaches. *Kalman v. Kimberly-Clark Corp.*, 713 F.2d 760, 218 U.S.P.Q. 781 (Fed. Cir. 1983). To anticipate a claim, a reference must disclose every element of the challenged claim and enable one skilled in the art to make the anticipating subject matter. *PPG Industries, Inc. v. Guardian Industries Corp.*, 75 F.3d 1558, 37 U.S.P.Q.2d 1618 (Fed. Cir. 1996).

**ii. 35 U.S.C. §102(b) rejection analysis**

The Examiner finally rejected claims independent claims 1 14 and 46 under 35 U.S.C 102(b) as being anticipated by Smith et al (US Pat. 6,046,897). The Examiner has asserted that the Smith et al. reference teaches every element of claims 1, 14 and 46.

Claims 1, 14, and 46 are as follows:

1. (Original) An electrostatic discharge protection circuit comprising:  
one or more electrostatic bus lines to direct electrostatic discharge around internal circuitry;

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a plurality of signal bonding pads to receive external voltage signals, each signal bonding pad is coupled to an associated electrostatic bus line via an unidirectional conducting device; and

a charge pump for each electrostatic bus line to precharge its associated electrostatic bus line to an associated predetermined voltage level, wherein pre-charging each electrostatic bus line to its predetermined voltage level reduces transient currents on the signal bonding pads associated with capacitive charging of the electrostatic bus lines when the external voltage signal levels are beyond normal supply voltage ranges.

14. (Original) An integrated circuit comprising:

functional circuitry;

a first electrostatic discharge (ESD) bus line to direct electrostatic discharge pulses away from the functional circuitry;

a first charge pump coupled to charge the first ESD bus line to a predetermined first voltage;

a second ESD bus line to further direct electrostatic discharge pulses away from the functional circuitry;

a second charge pump coupled to charge the second ESD bus line to a predetermined second voltage;

a first unidirectional conducting device coupled between a first signal connection and the first ESD bus line;

a second unidirectional conducting device coupled between a second signal connection and the second ESD bus line; and

wherein the first and second ESD bus lines are charged to their respective first and second voltage levels to reduce transient currents through the first and second unidirectional conducting devices when voltages applied to the first and second signal connections are outside the normal range of power supply operating voltages for the integrated circuit.

46. (Original)A method of operating an integrated circuit that requires signal voltages outside the

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normal range of operational power supply voltages, the integrated circuit including an electrostatic discharge circuit having one or more electrostatic discharge bus lines, the method comprising:

pre-charging each of the electrostatic discharge bus lines to a respective predetermined voltage level, wherein each predetermined voltage level is a voltage level beyond the signal voltage level expected to be applied to the integrated circuit.

In regards to claims 1 and 14, each of the independent claims include the element of a charge pump for each electrostatic discharge bus line. Each charge pump is adapted to charge its associated electrostatic discharge bus line to a predetermined voltage. The Smith et al. reference does not teach the use of charge pumps. The Examiner has asserted that diodes 810 and 816 of the Smith et al. reference are charge pumps. However, the passive diodes 810 and 816 are not the same as the active charge pumps 120 and 122 of the present application. An example of a charge pump of one embodiment of the present invention is illustrated in Figure 3 of the present application. As illustrated in Figure 3, the charge pump of the present invention is an active circuit that is capable of charging its associated ESD line to a predetermined voltage. The diodes 810 and 816 are passive devices that allow current to flow from VDD to a segmented ESD bus. Please see Figure 8 and column 12 lines 41-54. This is not what is disclosed or claimed in claims 1 or 14 of the present application. Since, a 35 U.S.C. § 102 rejection requires a single piece of art teach every element of a claim and the Smith et al. reference does not teach every element of claims 1 and 14, the Examiner erred in rejecting claims 1 and 14 under 35 U.S.C. § 102.

Regarding independent Claim 46, not every element of Claim 46 is taught by the Smith et al. reference. Claim 46 includes the element, “pre-charging each of the electrostatic discharge bus lines to a respective predetermined voltage level, wherein each predetermined voltage level is a voltage level beyond the signal voltage level expected to be applied to the integrated circuit.” Embodiments of the present invention, disclose an ESD protection scheme that can be used in

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ICs that occasionally operate above Vdd or below Vss. Please see Paragraphs [0005] and [0006] of the present invention. “When the ESD bus lines 45 and 47 are precharged to the desired voltages, steering diodes 10, 16, 20, 24, 40, 42, 44 and 46 remain in a reversed bias state during normal operations even if the voltage levels on the signal pads 14 and 22 are beyond the normal range of the supply voltages.” See paragraph [0033] of the present application. The Smith et al. reference relates to a segmented Bus architecture so that individual I/O pads may be reduced in size. Please see the Abstract of the Smith et al. reference. Diodes 810 and 816 of the Smith et al. reference allow current flow from VDD to the respective segmented EDS bus. Please see paragraph 12, lines 33-54 of the Smith et al. reference. However, the Smith et al. reference does not teach “pre-charging each of the electrostatic discharge bus lines to a respective predetermined voltage level, wherein each predetermined voltage level is a voltage level beyond the signal voltage level expected to be applied to the integrated circuit,” (emphasis added) as is disclosed and claimed in Claim 46 of the present application. Since not every element is taught by the Smith et al. reference a rejection under 102 was improper. Accordingly, the Applicant respectfully requests the withdrawal of the rejection of Claim 46 under 35 U.S.C. §102(b).

**C. Rejection of Claim 26 Under 35 U.S.C. § 103(a)**

**i. The Applicable Law**

35 U.S.C. § 103 provides in relevant part:

Conditions for patentability; non-obvious subject matter.

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter

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pertains. Patentability shall not be negated by the manner in which the invention was made.

"The ultimate determination . . . whether an invention is or is not obvious is a legal conclusion based on underlying factual inquiries including: (1) the scope and content of the prior art; (2) the level of ordinary skill in the prior art; (3) the differences between the claimed invention and the prior art; and (4) objective evidence of nonobviousness." *In re Dembiczak*, 175 F.3d 994, 998, 50 USPQ2d 1614, 1616 (1999) (citing *Graham v. John Deere Co.*, 383 U.S. 1, 17-18, 148 USPQ 459, 467 (1966)).

When applying 35 U.S.C. §103, the claimed invention must be considered as a whole; the references must be considered as a whole and must suggest the desirability and thus the obviousness of making the combination; the references must be viewed without the benefit of impermissible hindsight vision afforded by the claimed invention and a reasonable expectation of success is the standard with which obviousness is determined. *Hodosh v. Block Drug Co., Inc.*, 786 F.2d 1136, 1143 n.5, 229 USPQ 182, 187 n.5 (Fed. Cir. 1986).

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. MPEP 2143

The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. MPEP 2143 citing *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

**ii. 35 U.S.C. §103(a) rejection analysis**

The Examiner finally rejected independent Claim 26 under 35 U.S.C. §103(a) as being unpatentable over Smith et al. in view of Ker et al. Specifically, the Examiner asserted in the Final Office Action that:

Regarding independent Claim 26, not every element of Claim 26 is taught or suggested by the Smith et al. reference or the Ker et al. reference. For example, Claim 26 includes the element, “a positive rail charge pump coupled to charge the positive ESD bus line to a predefined voltage level.” Neither the Smith et al. nor the Ker et al. reference alone or in combination teach or suggest “a positive rail charge pump coupled to charge the positive ESD bus line to a predefined voltage level,” as is disclosed and claimed in Claim 14 of the present application. The Examiner cites 810 and 816 of the Smith et al. reference as a charge pump. However, 810 and 816 are described in the Smith et al. reference as passive diodes that merely allow current to flow from voltage supply VDD. Please See Column 12, lines 41-44 and lines 50-54 of the Smith et al. reference. This is not what is claimed in Claim 26 as reproduced above. Moreover, neither the Smith et al. nor the Ker et al. reference teach or suggest the element “wherein the predefined voltage level is higher than anticipated voltage signal levels that will be applied to the first signal bonding pad to reduce parasitic currents through the first unidirectional conducting device during normal operations of the integrated circuit where voltage signals higher than a normal power supply operating voltage, but less than the predefined voltage, are applied to the first signal bonding pad.” Since not every element is taught or suggested by the Smith et al. or the Ker et al. reference, a rejection under 103 was improper. Accordingly, the Applicant respectfully requests the withdrawal of the rejection of Claim 26 under 35 U.S.C. §103(a).

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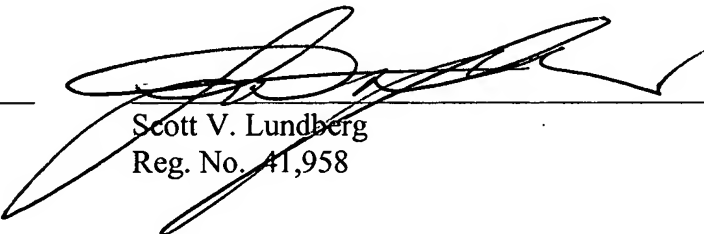
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**10. Summary**

Appellants have set forth reasons why the Examiner is incorrect in maintaining the rejections of the pending claims. Specifically, the Examiner has failed to set forth a prima facie case of anticipation or obviousness. Neither Smith et al. nor Ker et al. either alone or in combination teach all of the limitations in the pending independent and dependant claims. Appellant respectfully submits that, for the above reasons, Claims 1, 2, 4-16, 22, 26-31, 33, 34 and 46-48 are allowable over the cited art. Therefore, reversal of the Examiner's rejections is respectfully requested.

Respectfully submitted,

Date: 5-11-04



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## **Appendix 1**

### **Claims on Appeal**

1. (Original) An electrostatic discharge protection circuit comprising:
  - one or more electrostatic bus lines to direct electrostatic discharge around internal circuitry;
  - a plurality of signal bonding pads to receive external voltage signals, each signal bonding pad is coupled to an associated electrostatic bus line via an unidirectional conducting device; and
  - a charge pump for each electrostatic bus line to precharge its associated electrostatic bus line to an associated predetermined voltage level, wherein pre-charging each electrostatic bus line to its predetermined voltage level reduces transient currents on the signal bonding pads associated with capacitive charging of the electrostatic bus lines when the external voltage signal levels are beyond normal supply voltage ranges.
2. (Original) The electrostatic discharge protection circuit of claim 1, wherein each electrostatic bus line is pre-charged to a voltage level beyond a normal supply voltage range.
4. (Original) The electrostatic discharge protection circuit of claim 1, wherein each unidirectional conducting device comprises:
  - a steering diode coupled to steer the electrostatic discharge away from the internal circuitry, wherein the pre-charging of an associated electrostatic bus line causes the steering diode to remain reversed biased even if voltages on associated signal bonding pads are beyond the normal supply voltage range and below a predetermined voltage range.
5. (Original) The electrostatic discharge protection device of claim 4, wherein the steering diode is a rectifier diode.

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6. (Original) The electrostatic discharge protection device of claim 4, wherein the steering diode is a Schottky diode.

7. (Original) The electrostatic discharge protection device of claim 1, wherein each unidirectional conducting device comprises:

a junction of a bipolar junction transistor.

8. (Original) The electrostatic discharge protection device of claim 7, wherein the bipolar junction transistor is formed with in a complementary metal-oxide semiconductor (CMOS) N well structure.

9. (Original) The electrostatic discharge protection device of claim 7, wherein the bipolar junction transistor is formed in a CMOS P well structure.

10. (Original) The electrostatic discharge protection device of claim 1, further comprising:  
a switching device coupled to each electrostatic bus line to selectively pass electrostatic pulses from one of the bonding pads to another of the bonding pads.

11. (Original) The electrostatic discharge protection device of claim 10, wherein the switching device comprises:

a bipolar junction transistor coupled to switch in response to the electrostatic pulses.

12. (Original) The electrostatic discharge protection device of claim 10, wherein the switching device comprises:

a MOSFET coupled to switch in response to the electrostatic pulses.

13. (Original) The electrostatic discharge protection device of claim 10, wherein the switching device comprises:

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a zener diode.

14. (Original) An integrated circuit comprising:

functional circuitry;

a first electrostatic discharge (ESD) bus line to direct electrostatic discharge pulses away from the functional circuitry;

a first charge pump coupled to charge the first ESD bus line to a predetermined first voltage;

a second ESD bus line to further direct electrostatic discharge pulses away from the functional circuitry;

a second charge pump coupled to charge the second ESD bus line to a predetermined second voltage;

a first unidirectional conducting device coupled between a first signal connection and the first ESD bus line;

a second unidirectional conducting device coupled between a second signal connection and the second ESD bus line; and

wherein the first and second ESD bus lines are charged to their respective first and second voltage levels to reduce transient currents through the first and second unidirectional conducting devices when voltages applied to the first and second signal connections are outside the normal range of power supply operating voltages for the integrated circuit.

15. (Original)The integrated circuit of claim 14, wherein the first unidirectional conducting device is a diode having a cathode terminal coupled to the first ESD bus line and an anode terminal coupled to the first signal connection.

16. (Original)The integrated circuit of claim 14, wherein the second unidirectional conducting device is a diode having a cathode terminal coupled to the second signal connection and an anode terminal coupled to the second ESD bus line.

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17-21. (Objected to)

22. (Original) The integrated circuit of claim 14, further comprising:

a switching device coupled between the first and second ESD bus lines, the switching device is switchable between a high impedance and low impedance state.

23-25. (Objected to)

26. (Original) An ESD protected integrated circuit comprising:

a positive ESD bus line to route positive electrostatic discharge pulses around functional circuitry;

first and second signal bonding pads to receive external voltage signals;

a first unidirectional conducting device coupled between the first signal bonding pad and the positive ESD bus line;

a second bus line coupled to selectively receive current from the positive ESD bus line;

a second unidirectional conducting device coupled between the second signal bonding pad and the second bus line; and

a positive rail charge pump coupled to charge the positive ESD bus line to a predefined voltage level, wherein the predefined voltage level is higher than anticipated voltage signal levels that will be applied to the first signal bonding pad to reduce parasitic currents through the first unidirectional conducting device during normal operations of the integrated circuit where voltage signals higher than a normal power supply operating voltage, but less than the predefined voltage, are applied to the first signal bonding pad.

27. (Original) The ESD protected integrated circuit of claim 26, wherein the second unidirectional conducting device comprises a diode.

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28. (Original)The ESD protected integrated circuit of claim 26, further comprising:

a supply clamp to selectively conduct current from the positive ESD bus line to the second bus line when a positive electrostatic discharge pulse is detected, the supply clamp is coupled between the positive ESD bus line and the second bus line.

29. (Original)The ESD protected integrated circuit of claim 26, wherein each of the first and second unidirectional conducting devices comprise a diode.

30. (Original)The ESD protected integrated circuit of claim 29, wherein the predefined voltage level keeps the diodes in a reverse bias state during normal operation.

31. (Original)The ESD protected integrated circuit of claim 26, wherein the first unidirectional conducting device comprises a transistor.

32. (Objected to)

33. (Original)The ESD protected integrated circuit of claim 31, wherein the transistor is formed in a N well CMOS structure.

34. (Original)The ESD protection integrated circuit of claim 33, wherein the N well CMOS structure further comprises:

a N type conductivity well formed in a P type conductivity substrate of the integrated circuit;

a N type conductivity base formed by the well;

a P type conductivity emitter with high dopant density formed in the well; and

a P type conductivity collector formed by the substrate.

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35. (objected to)

36-45 (Allowed)

46. (Original)A method of operating an integrated circuit that requires signal voltages outside the normal range of operational power supply voltages, the integrated circuit including an electrostatic discharge circuit having one or more electrostatic discharge bus lines, the method comprising:

pre-charging each of the electrostatic discharge bus lines to a respective predetermined voltage level, wherein each predetermined voltage level is a voltage level beyond the signal voltage level expected to be applied to the integrated circuit.

47. (Original)The method of claim 46, wherein pre-charging the electrostatic discharge bus lines prevents parasitic current from flowing through unidirectional conducting devices when signal voltages are applied to the integrated circuit that are outside the normal range of operating power supply voltages during operation of the integrated circuit.

48. (Original)The method of claim 46, wherein an electrostatic bus line is pre-charged to a voltage level higher than an expected positive voltage signal.

49. (Objected to)

50-57. (Allowed)